***Original Research Article***

# Addressing Package Voids on Extremely Small Leadframe Device


## ABSTRACT

The paper focused in addressing the package voids defect of a semiconductor device utilizing an extremely small leadframe technology. Potential risk analysis and pareto diagram were completed to identify the top reject contributors and eventually come-up with the robust solution. A comprehensive design of experiments (DOE) was done and solution validation was employed to formulate the effective corrective actions. Results revealed that package voids were addressed by optimizing the molding process focusing on the molding temperature and curing time. A significant improvement of 95 % for package voids reduction was achieved. For future works, the parameters and learnings could be used on devices with similar configuration.



*Keywords: Mold process; package voids; leadframe; semiconductor; compression molding.*


## 1. INTRODUCTION

New trends and continuous development in semiconductor technology offer great challenges in assembly manufacturing industry. An imperative challenge for any industry is to maintain its competitive market position and value. Important to note that failure to provide customer expectation in terms of quality and time-to-market would result to possible business failure. This critical scenario should realty be avoided that is why a line-stressing or risk production is being employed in preparation to full or mass production mode.

The device in focus is a newly-introduced leadframe package in the plant having an extremely small footprint as illustrated in Fig. 1. The device functions as a diode with a single wire connection, for mobile phones and computer applications. Regardless of its simple geometry, it is considered as a device with high complexity as state-of-the-art platforms are needed to satisfy its output process.


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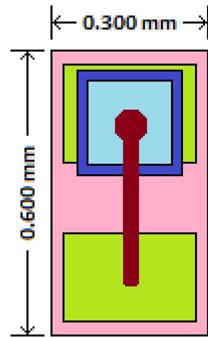


**Fig. 1. Device dimension**

The device has a very thin die and with the smallest total package dimension. The assembly manufacturing process includes a step cutting method of wafers, compression molding, and in-strip testing, which are not common on other semiconductor industries. A part of the assembly process flow is shown in Fig. 2. Worthy to note that assembly and test process flow varies with the product and the technology [1-3]. With the continuing technology trends and state-of-the-art platforms, challenges in semiconductor assembly manufacturing are inevitable [4-7].

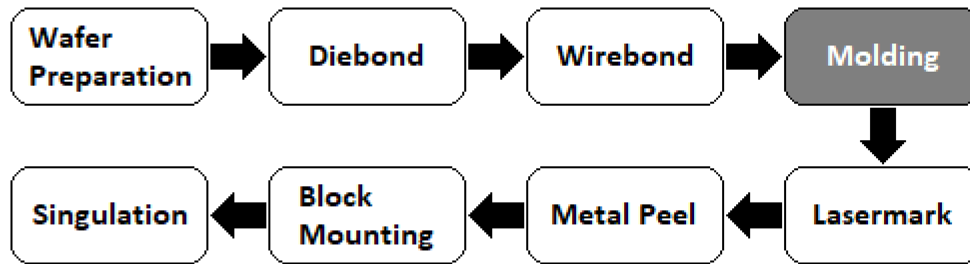


**Fig. 2. Assembly process flow**

Delinquency in view of customer was the scenario encountered during the line-stressing and ramp-up of the device. Critical processes were identified using risk analysis, and one of which is identified in Table 1 that focused on the molding process. Evaluation was made before the risk build to accelerate confidence on line-stressing. Furthermore, potential risk analysis was given contingency plans and created corrective actions.

**Table 1. Potential risk analysis at molding process**

| Identified risk | Resulting potential risk | Evaluation before action | | | Identified action |
|---|---|---|---|---|---|
| | | Probability | Impact | Class | |
| 0.3 mm package molding, package molding defects, voids, incomplete fill | ▪Low yield<br>▪Reliability | 9 | 9 | A | Capability using compression molding technology |

Reject contributors on the identified critical processes are shown in Fig. 3. Molding is one critical process identified with deviations or output abnormalities as a result of un-optimized parameters which are normally attributed to newly-introduced devices.

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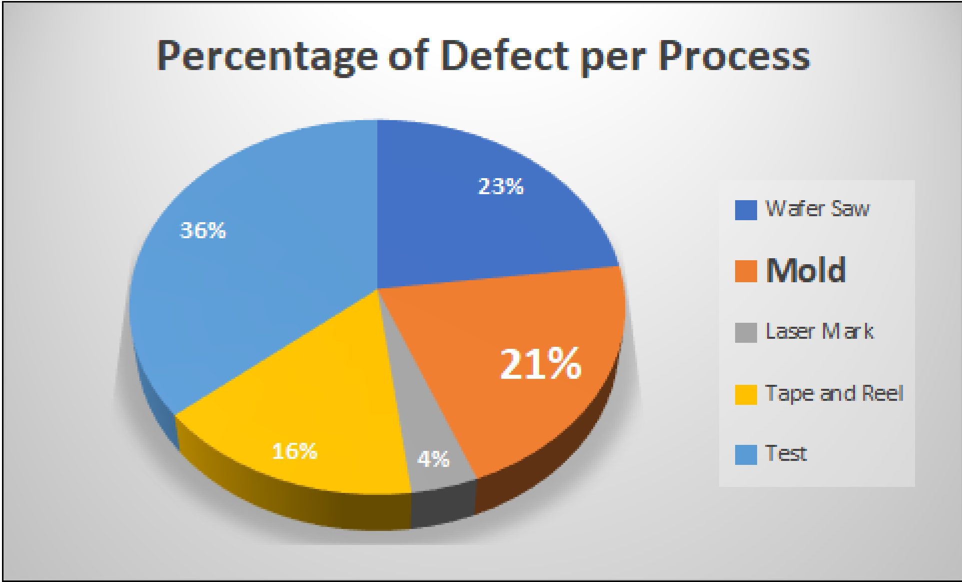



**Fig. 3. Defect contribution per assembly process**

Of the 21 % defect contribution of the molding process, pareto diagram in Fig. 4 shows package voids as the top reject parts per million (ppm) contributor. Parameter optimization is one of the factors to be checked as the device in focus has no other similar product in the plant as reference. Benchmarking for similar device from other sites is being considered to have a baseline for critical process parameters.

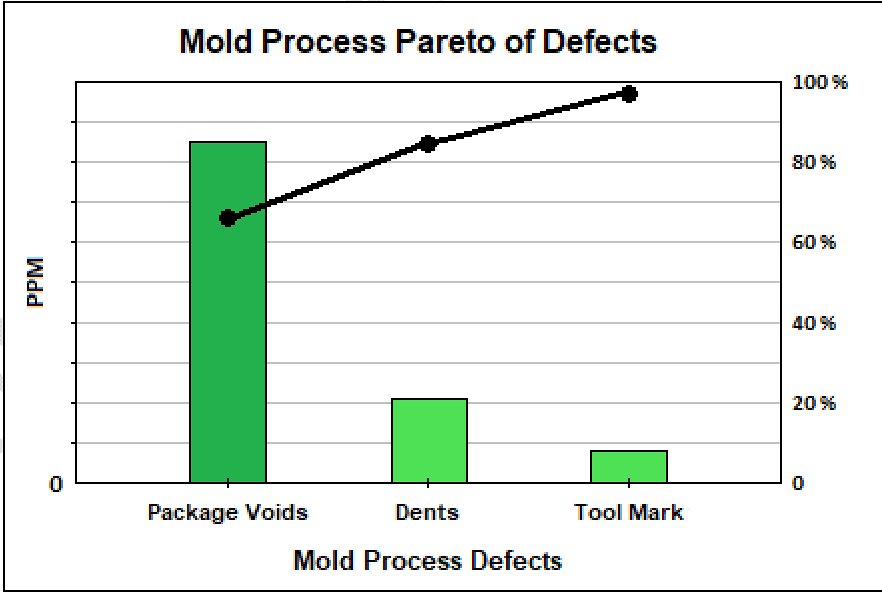
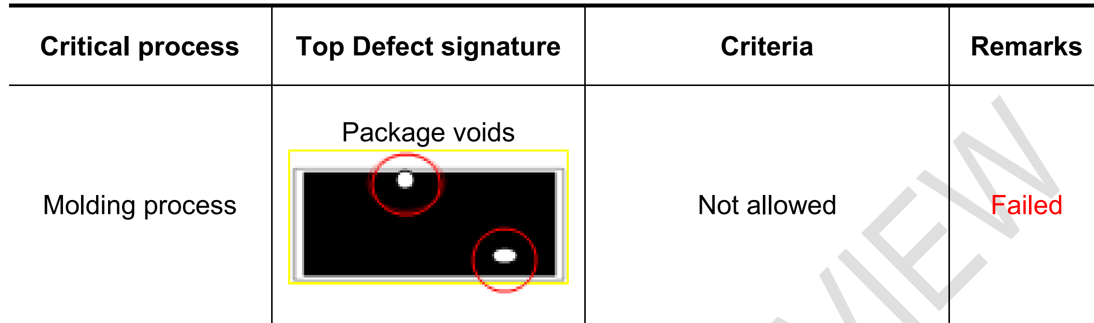



**Fig. 4. Pareto diagram of mold process rejects highlighting the top contributor**

Top rejects based on pareto diagram substantially affect the yield and delivery during production stressing performance. Henceforth, process optimization is highly recommended

at line-stressing before it reaches the full-production release. Table 2 shows the top defect signature of the molding saw process. Further analysis and investigation of failures were employed by collecting the actual reject samples at this critical process, which are essential in formulating the corrective actions and improvement.

**Table 2. Top defect signature of molding process**



| Critical process | Top Defect signature | Criteria | Remarks |
|---|---|---|---|
| Molding process | Package voids | Not allowed | Failed |

## 2. LITERATURE REVIEW

One of the integral components in the production of semiconductor devices is the molding compound, a packaging material for encapsulation to protect the device from external environment [8]. Th device uses compression molding shown in Fig. 5 and with ultra-fine filler compound.

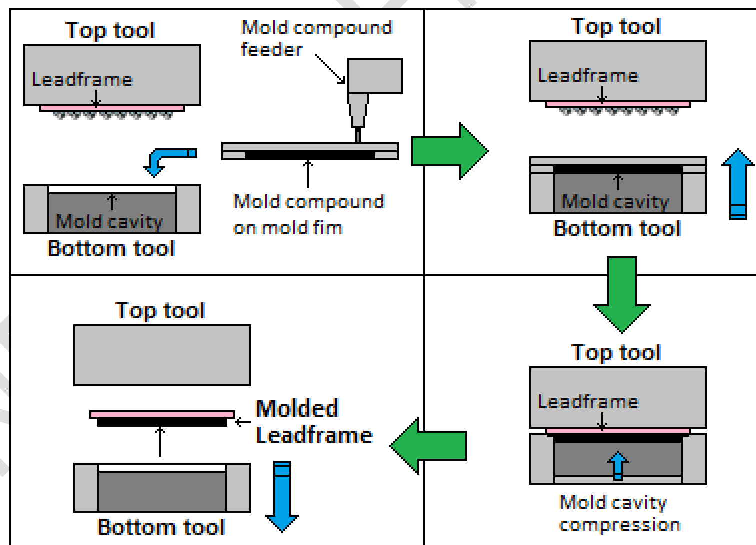



**Fig. 5. Compression molding mechanism**

The advantages of compression molding system are zero/less wire damage, good filling on narrow gap on die, and no cull/no runner. The technology was necessary for SPPD due to the requirement of narrow mold thickness. With this, device is prone to voids during molding, thus voids became the top reject contributor. Mold voids are commonly easy to correct, but this requires a thorough parameter optimization through design of experiments (commonly referred as DOE). DOE was done to achieve desired parameter range for

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molding process considering the critical input and output responses. Moreover, package voids is the critical and primary output response.

## 3. METHODOLOGY

DOE for compression mold was conducted with the objective to determine and define window for critical parameter range, thus eliminate mold voids. Shown in Fig. 6 is the DOE matrix prepared using a statistical software that automatically provides the combination of runs.

3x3 Factorial
Design 3x3 Factorial
Screening
Model
Columns (4/0)
Pattern
MOLD TEMP
CURE TIME
MOLD VOIDS

| | Pattern | MOLD TEMP | CURE TIME | MOLD VOIDS |
|---|---|---|---|---|
| 1 | 11 | 170 | 160 | • |
| 2 | 22 | 175 | 180 | • |
| 3 | 12 | 170 | 180 | • |
| 4 | 13 | 170 | 200 | • |
| 5 | 23 | 175 | 200 | • |
| 6 | 32 | 180 | 180 | • |
| 7 | 21 | 175 | 160 | • |
| 8 | 33 | 180 | 200 | • |
| 9 | 31 | 180 | 160 | • |

**Fig. 6. DOE evaluation matrix**

Full factorial design with a total of nine runs was created. Using the statistical software tool, mold temperature and cure time were identified as the most critical parameters that will cause mold voids defect. Results of each run are discussed in the succeeding section.

## 4. RESULTS AND DISCUSSION

During development, the initial problem encountered was package voids every shot. Together with the mold machine field support and the mold compound technical support, DOE was performed using a matrix of different batches of mold compound and sets of mold parameters. The DOE result is illustrated in Fig. 7.

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| Molding type | | Transfer Mold | Compression Mold | | | |
|---|---|---|---|---|---|---|
| Sample name | | - | Sample-2 | - | - | - |
| EMC name | | 9240ZHF10 (Zx2.5) | 9240ZHF10W (GTL,S) | 9240ZHF10W (GTL,A) | 9240ZHF10W -30 | 9240ZHF10W -45 |
| Epoxy Resin | - | MA/ Biphenyl | | | | |
| Hardener | - | LWA-1 | | | | |
| Wax | - | Current | Reduced amount | | | |
| Catalyst content | - | Current | Reduced amount | | | |
| Flame retardant | - | No | | | | |
| Anti bubble agent "S" | - | No | Yes | Increased | Yes | |
| Z flexibilizer | - | Yes (x2.5) | | | | |
| Filler Content | vol%/wt% | 80/89 | | | | |
| Filler shape | - | All spherical | | | | |
| | | 75um cut | | | 30um cut | 45um cut |
| Powder sieving | - | No | 150um on 1mm pass | | | |
| Spiral flow | inch | 33 | 55 | 55 | 50 | 53 |
| Flash length | mm | 1.1 | 1.7 | 1.7 | 1.7 | 1.4 |
| Hot hardness(90sec) | - | 88 | 72 | 72 | 63 | 56 |
| Gelation time(175C) | sec | 32 | 75 | 90 | 102 | 93 |
| Viscosity(175C) | poise | 230 | 140 | 140 | 250 | 270 |
| Disk flow | mm | 78 | 94 | 94 | 91 | 91 |
| Tg | degC | 135 | 135 | 135 | 130 | 125 |
| CTE alpha-1 | ppm/C | 8 | 7 | 7 | 8 | 7 |
| CTE alpha-2 | ppm/C | 30 | 27 | 27 | 30 | 27 |
| Flexural Modulus | kgf/mm2 | 2400 | 2400 | 2400 | 2500 | 2500 |
| Flexural Strength | kgf/mm2 | 15 | 14 | 15 | 15 | 15 |
| Water absorption | % | 0.23 | 0.23 | 0.23 | 0.27 | 0.28 |
| Mold shrinkage | % | 0.06 | 0.06 | 0.06 | 0.05 | 0.11 |

MA: Multi Aromatic Type
LWA-: Low Water Absorption Type 1
MF: Multi Funtional Type

Need longer cure time such as 175degC/180sec

To reduce surface voids

**Fig. 7. DOE matrix for compression molding process optimization**

DOE results of compression molding showed that optimum parameters in terms of package voids can be achieved by using the 175°C and 180 seconds curing time regardless of molding compound used.

After the implementation of the identified solutions, level of rejections was monitored. Fig. 8 shows the improvement in the ppm level, before and after the solution implementation. Actual ppm values are intentionally not shown due to confidentiality.

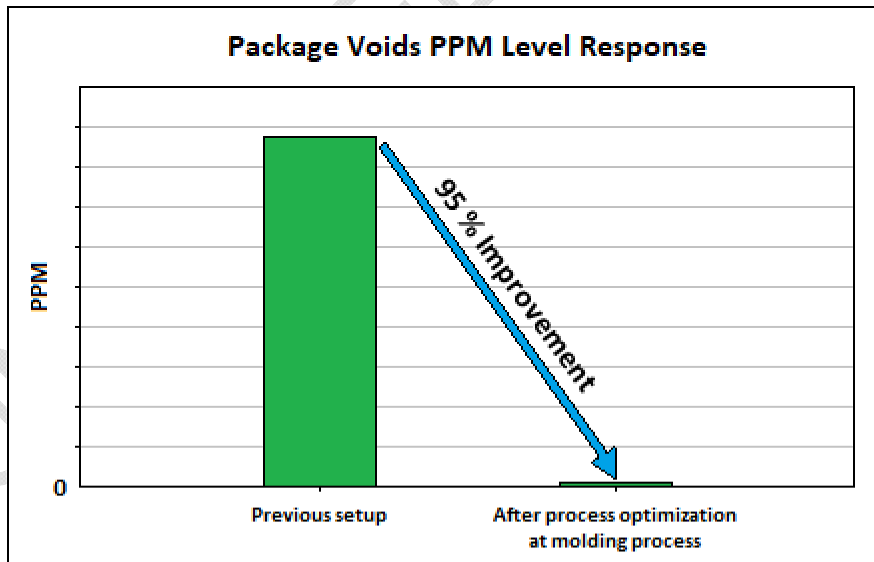


**Fig. 8. Improvement after optimization and implementation of corrective actions**

An improvement of 95 % for die chippings reduction was achieved through the comprehensive DOE. Assembly yield trend stabilized after the implementation, optimization, and sustainability of the improvement and all corrective actions. This is a good indication of manufacturing preparedness for full-production mode.

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## 5. CONCLUSION AND RECOMMENDATIONS

Comprehensive engineering analyses with the aid of statistical analysis were done in solving and addressing the package voids of an extremely small device at molding process. Through DOE, parameters optimization was formulated, with package voids occurrence significantly minimized by achieving the optimum molding temperature and curing time. A 95 % improvement for package voids reduction was ultimately achieved.

Process optimization plays a vital role to as early as line-stressing stage, before full-production release can be granted. It is important that when newly-introduced devices are coming in, critical processes should be identified and that appropriate improvement, corrective actions, and solutions be made so that when full-production is set, both quality and speed would be achieved. Techniques and learnings shared in this paper could be used for future works on semiconductor devices with comparable configuration.

## COMPETING INTERESTS DISCLAIMER:

Authors have declared that no competing interests exist. The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

## REFERENCES

1. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; May 2006.
2. Nenni D, McLellan P. Fabless: the transformation of the semiconductor industry. CreateSpace Independent Publishing Platform, USA; April 2014.
3. Harper C. Electronic packaging and interconnection handbook. 4th ed., McGraw-Hill Education, USA; October 2004.
4. Tsukada Y, Kobayashi K, Nishimura H. Trend of semiconductor packaging, high density and low cost. Proceedings of the 4th International Symposium on Electronic Materials and Packaging. Taiwan. 2002;1-6.
5. Lay Yeap L. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
6. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore. 2008;1-11.
7. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
8. Ardebili H, Zhang J, Pecht M. Encapsulation technologies for electronic applications. 2nd ed., William Andrew Applied Science Publishers, Elsevier, USA; October 2018.

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