RF Matching Networks Using S-Parameters

Frederick Ray I. Gomez[1*]

[1]New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna, Philippines 4027

.

ABSTRACT

The paper presents a design and study of impedance matching for radio frequency (RF) circuit application of common-source amplifier topology. Matching networks for input and output sides of the amplifier were determined from the S-parameters given for the transistor at frequency of 2.6 GHz and ensuring unconditional stability requirement. Impedance matching is necessary in RF circuit design to provide maximum possible power transfer between the source and the load. Two designs were modeled, simulated, and analyzed employing L-network input and output matching networks. The design with inductor-capacitor combination in the L-matching networks exhibited a stable and smoother behavior for higher frequencies compared to an all-inductor design. Complex tradeoffs among technology specifications and design parameters are inevitable, therefore should be carefully handled in designing the impedance matching networks, to optimize the performance of the common-source amplifier. Ultimately, the common-source amplifier achieved a gain of 6.569 dB at 2.6 GHz. For future research, physical implementations of the impedance matching networks could be studied in order to improve and optimize the simulated models.

Keywords: Impedance matching, S-parameters; common-source amplifier; reactance.

1. INTRODUCTION

Impedance matching plays vital role in optimizing the performance of the radio frequency (RF) integrated circuit design. Matching provides maximum power transfer between the input or source and the output or the load, thus allowing the RF circuit to achieve the desired performance esp. the gain requirements. Passive elements such as inductors and capacitors are vital for impedance matching and are specifically designed such that they would satisfy the gain requirements at a specific frequency or range of operation [1-5]. Design tradeoffs between matching network parameters are inevitable, so it is crucial that inductors and capacitors be designed carefully for the specific requirements of the intended application.

For this study, a common-source amplifier is analyzed and optimized using impedance matching. Common-source amplifier shown in Fig. 1 is one of three basic topologies of single-stage transistor amplifier, typically used as a voltage amplifier for RF applications. It exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom [3-6]. The input signal is fed into the gate (g) terminal of the transistor. The output is produced at the drain (d) terminal, while the source (g) terminal is what is known as “common” and for this one connected to a ground. As earlier mentioned, one way to optimize the performance of the common-source amplifier is to employ impedance matching which will be the focus of this paper.

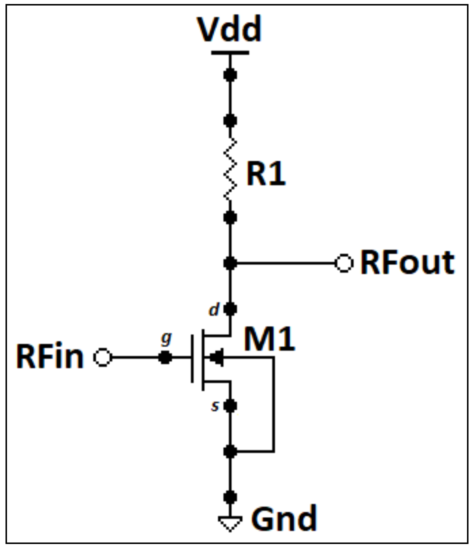

Fig. 1. Schematic diagram of common-source amplifier

2. LITERATURE REVIEW

Impedance matching at input and/or output sides of the circuit could reinforce the performance improvement and optimization of the designed amplifier. Matching offers maximum power transfer between the input or source and the output or the load, thus allowing the common-source amplifier to achieve the desired performance esp. the gain requirements [4-5]. Maximum power transfer is achieved when both the generator and load are conjugately matched to the two-port network, as depicted in Fig. 2 block diagram.

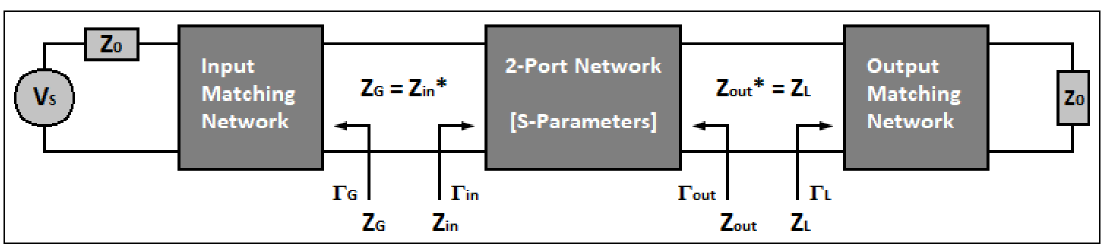

Fig. 2. Two-port network with matching networks [4]

Where

Γ_{in} = input reflection coefficient of the two-port network

Γ_{out} = output reflection coefficient of the two-port network

Γ_G = source or generator reflection coefficient

Γ_L = load reflection coefficient

Z_{in} = input impedance of the two-port network

Z_{out} = output impedance of the two-port network

Z_G = source or generator impedance

Z_L = load impedance

The generator/source and load reflection coefficients could be derived using the computed stability values earlier discussed.

$$\Gamma_G = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad (1)$$

$$\Gamma_L = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (2)$$

With the expressions in (1) and (2), generator and load impedances could now be obtained.

$$Z_G = \left(\frac{1+\Gamma_G}{1-\Gamma_G}\right) Z_0 \quad (3)$$

$$Z_L = \left(\frac{1+\Gamma_L}{1-\Gamma_L}\right) Z_0 \quad (4)$$

The expressions are critical for determining the reflection coefficients and impedance, which are computed in the succeeding section.

3. METHODOLOGY

Actual S-parameters of a common-source amplifier with transistor of width = 300 µm and length = 0.25 µm were initially given for this particular study. Required values of scattering parameters (hereinafter referred to as S-parameters) for a specific frequency of operation could then be determined using linear interpolation. S-parameters of the transistor are given in Table 1 at frequency initially set to 2.6 GHz.

Table 1. S-parameters at frequency of 2.6 GHz

S-Parameters	Real part	Imaginary part
S11	0.59986	-0.53991
S21	-0.21942	1.14183
S12	0.06752	0.03731
S22	0.11658	-0.40044

Stability conditions of the two-port network in terms of S-parameters play an essential role in amplifier designs. Although stability is frequency dependent, we want to ensure that the amplifiers design exhibits unconditional stability esp. at higher frequencies. Expressions of stability constants discussed in [4] could be used to check for the stability of the common-source amplifier design. Computed constants in Table 2 are then used to compute for the source/generator and load reflection coefficients.

Table 2. Computed stability constants

Stability constants	Values

Δ	0.38253 ∢-103.43°
K	1.78957
B1	1.33106
B2	0.37628
C1	0.65208 ∢-44.98°
C2	0.13295 ∢-103.49°

To have unconditional stability, the Rollett stability factor (K) must be greater than unity (1), that is, K > 1, as well as one other condition given in [4-5]. Computations (not shown) observed that all of the conditions are met. With this, the two-port network in terms of S-parameters is unconditionally stable. Shown in Table 3 are the values of the computed reflection coefficients and impedances, assuming normalized impedance of Z_0 = 50 Ω.

Table 3. Reflection coefficients and impedance values

Γ and Z	Values
Γ_{in}	0.57750 - j0.57717
Γ_{out}	-0.09650 - j0.40242
Γ_G	0.57750 + j0.57717
Γ_L	-0.09650 + j0.40242
Z_{in}	32.57934 - j112.81061 Ω
Z_{out}	30.37350 - j29.49728 Ω
Z_G	32.57934 + j112.81061 Ω
Z_L	30.37350 + j29.49728 Ω

L-network is used for the input and output matching networks in Figs. 3-4 since it is the simplest and most widely used matching network for lumped elements.

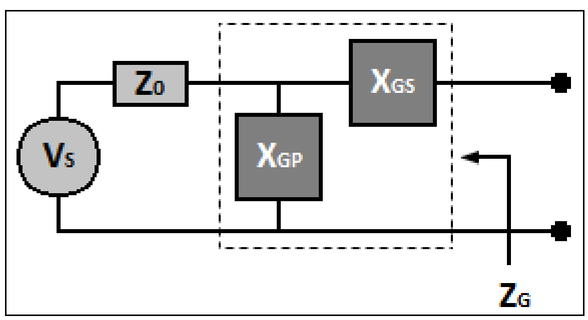

Fig. 3. L-network of the input matching network [4]

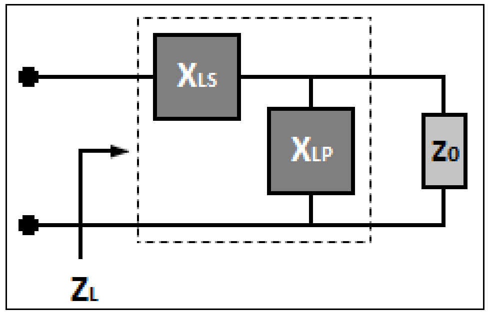

Fig. 4. L-network of the output matching network [4]

Where

X_{GS} = series reactance of the L-network of the input matching network

X_{GP} = parallel reactance of the L-network of the input matching network

X_{LS} = series reactance of the L-network of the output matching network

X_{LP} = parallel reactance of the L-network of the output matching network

The elements of the L-network for both the input and output matching network are arranged in such orientation given that the real components of Z_G and Z_L are smaller than the real component of the normalized impedance which is Z_0 = 50 Ω (R_0 = 50 Ω) [4-5]. Finally, Table 4 summarizes the computed values obtained for the reactances and the quality-factor (Q_G, Q_L).

Table 4. L-network elements

Q and Z	Values
Q_G	0.73124
X_{GP1}	68.37681 Ω
X_{GP2}	-68.37681 Ω
X_{GS1}	88.98723 Ω
X_{GS2}	136.63400 Ω
Q_L	0.80385
X_{LP1}	62.20081 Ω
X_{LP2}	-62.20081 Ω
X_{LS1}	5.08159 Ω
X_{LS2}	53.91296 Ω

Passive components particularly capacitors and inductors could be determined from the L-network reactances given the frequency of 2.6 GHz. Positive reactance implies an inductive component while a negative reactance denotes a capacitive component.

Two sets of passive component values are used in the design simulation to check if the whole circuit is actually matched at the frequency of operation. Design1 is composed of Lgs1 and Lgp1 for the input matching network and Lls1 and Llp1 for the output matching network. Design2 is comprised of Lgs2 and Cgp2 for the input matching network and Lls2 and Clp2 for the output matching network. Tables 5 shows the actual values computed.

Table 5. Actual L-network passive components

Passive components	Values
Lgp1	4.186 nH
Cgp2	0.895 pF
Lgs1	5.447 nH
Lgs2	8.364 nH
Llp1	3.808 nH
Clp2	0.984 pF
Lls1	0.311 nH
Lls2	3.300 nH

4. RESULTS AND DISCUSSIONS

Two designs were studied and simulated using the two sets of values of the input and output matching networks employing the L-network confiugration. Figs. 5-6 shows the schematic designs of Design1 and Design2. Figs. 7-10 shows the comparison of the results of the S-parameter plots of the two designs.

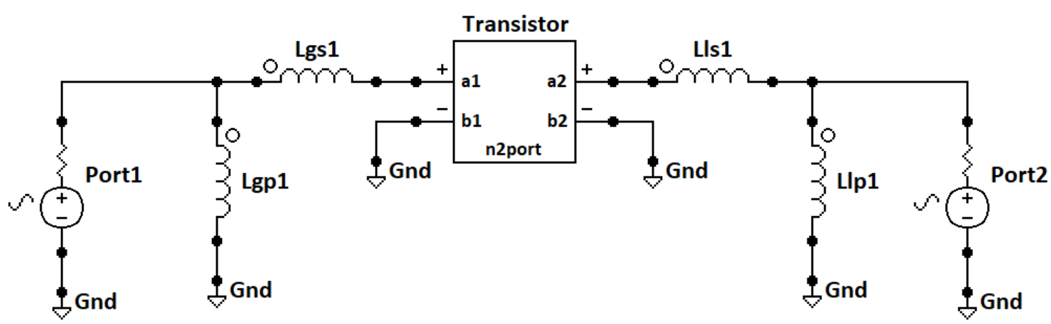

Fig. 5. Design1 schematic with all-inductor L-network configuration

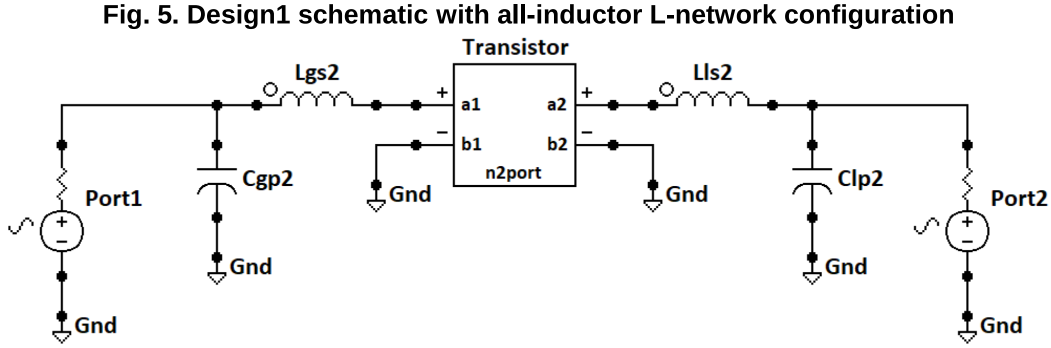

Fig. 6. Design2 schematic with inductor-capacitor L-network configuration

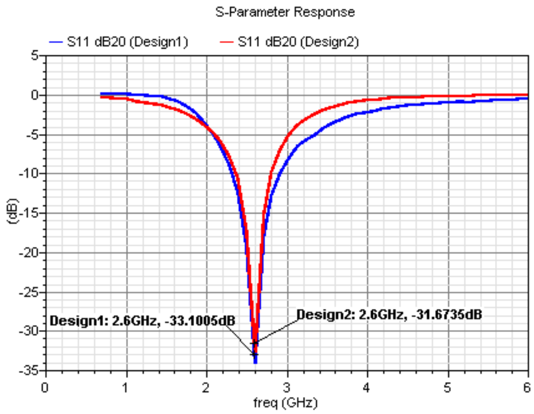

Fig. 7. S11 response in dB vs. frequency

Fig. 8. S21 response in dB vs. frequency

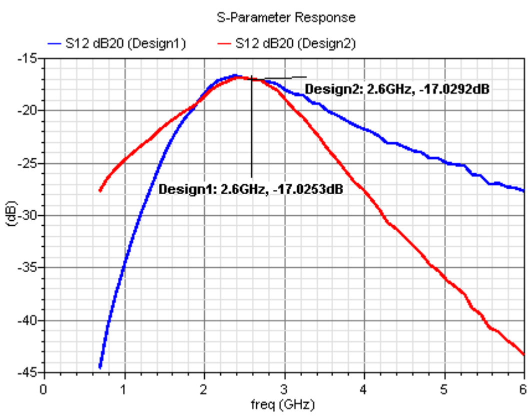

Fig. 9. S12 response in dB vs. frequency

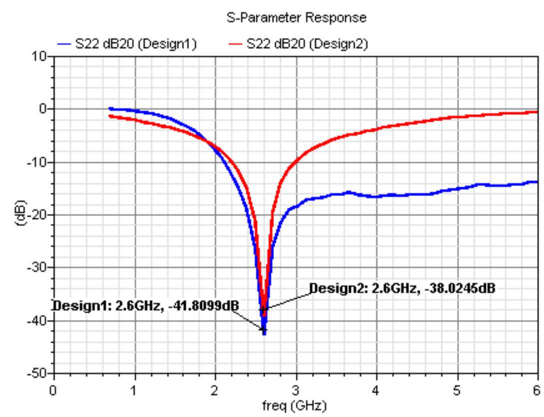

Fig. 10. S22 response in dB vs. frequency

The plots showed that the two designs are somehow matched at 2.6 GHz frequency, with values comparable and relatively close to each other. However, it can be observed that the S-parameter plots of Design2 are smoother than the plots of Design1 at frequencies greater than 2.6 GHz. The difference is evident esp. in the S22 plot in Fig. 10. This signifies that Design2, which is consist of inductor-capacitor combination in the L-matching networks, exhibits a stable behavior for higher frequencies than the Design1 which is an all-inductor design. Furthermore, the S11 and S22 plots of Design2 are more symmetric in reference to 2.6 GHz compared to the Design1. Table 6 summarizes the values of S-parameters at the frequency of operation.

Table 6. S-parameters response at 2.6 GHz

S-Parameters	Design1	Design2
S11	-33.101 dB	-31.674 dB
S21	6.573 dB	6.569 dB
S12	-17.025 dB	-17.029 dB
S22	-41.810 dB	-38.025 dB

The gain of the transistor or the common-source amplifier is indicated by the S21 plot. At 2.6 GHz, the gain is 6.573 dB and 6.569 dB for Design1 and Design2, respectively. It can be observed in the S21 plots that as the frequency increases in the higher frequencies esp. beyond the frequency of operation, the gain decreases. If the gain-bandwidth product is to be remained constant, then as the bandwidth or the frequency increases, the gain should compensate, thus decreasing the gain.

5. CONCLUSION AND RECOMMENDATIONS

Impedance matching is necessary in RF circuit design to provide maximum possible power transfer between the generator or source and the output load. Matching networks for input and output sides of the common-source amplifier were determined based on the S-parameters given for the transistor. Ensuring unconditional stability of the matching networks, two design models were considered and analyzed. Design2 which comprised of an inductor-capacitor combination in the input and output matching networks resulted to a smoother response or a more stable behavior at higher frequencies than the Design1 with all inductors in the matching networks. To optimize the performance of the RF circuit particularly the common-source amplifier, complex tradeoffs among technology specifications and design parameters should be carefully considered and analyzed in designing the impedance matching networks. The common-source amplifier achieved a gain of 6.573 dB and 6.569 dB for the two designs analyzed, respectively.

Design and study of passive elements could be helpful in understanding and optimizing the matching networks. Few software tools are available for such study [7-10]. For future works, actual or physical implementations of the impedance matching networks could be studied in order to further improve and optimize the simulated models.

ACKNOWLEDGMENT

The author would like to express gratitude to the New Product Development & Introduction (NPD-I) team and the Management Team for the utmost support. The author is greatly thankful to Prof. MT De Leon for the technical support.

REFERENCES

1. Razavi B. Phase-locking in high-performance systems: from devices to architectures. 1st ed., John Wiley & Sons, Inc., USA; 2003.
2. Long JR, Copeland MA. The modeling, characterization, and design of monolithic inductors for silicon RF IC's. IEEE Journal of Solid-State Circuits, vol. 32, no. 3; March 1997.
3. Baker RJ. CMOS: circuit design, layout, and simulation. 4th ed., Wiley-IEEE Press, USA; July 2019.
4. Bowick C, Ajluni C, Blyler J. RF circuit design. 2nd ed., Newton, Massachusetts, USA: Newnes, November 2007.
5. Razavi B. Design of analog cmos integrated circuits. 1st ed., McGraw-Hill Education, USA; August 2000.
6. Gray PR, Hurst PJ, Lewis SH, Meyer RJ. Analysis and design of analog integrated circuits. 5th ed., John Wiley & Sons, Inc., USA; January 2009.
7. Niknejad AM, Meyer RG. ASITIC for Windows NT/2000. Research in RFIC design. http://rfic.eecs. berkeley.edu/~niknejad/Asitic/grackle/cygwin_info.html
8. Niknejad AM, Meyer RG. Analysis and optimization of monolithic inductors and transformers for RF ICs. in Proc. IEEE Custom Integrated Circuits Conference, USA, pp. 375-378; May 1997.

9. Stanford Microwave Integrated Circuits Laboratory. Integrated spiral inductor calculator. http://www-smirc. standford.edu/spiralCalc.html
10. Gomez FR. A Fundamental approach for design and optimization of a spiral inductor. Journal of Electrical Engineering, David Publishing Co., vol. 6, no. 5, pp. 256-260; September 2018.